

AMD Athlon 2000 Update

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AMD Strategy

- ◆ Offer x86 solutions that span top to bottom the PC market
- ◆ Move beyond our success in the consumer desktop/mobile markets and grow market share in commercial desktops, servers and workstations
- ◆ Maintain competitive frequency roadmap with migration to 0.18um aluminum and copper technologies
 - ◆ Multiple AMD Athlon™ processor core derivatives to address different markets
 - ◆ 1GHz Athlon processor in 2000
- ◆ Deploy advanced technology
 - ◆ LDT (high-performance I/O bus)
 - ◆ SledgeHammer (AMD's 8th Generation Processor)
- ◆ Continued emphasis on Infrastructure, Customer & Channel Partnerships



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Manufacturing Update

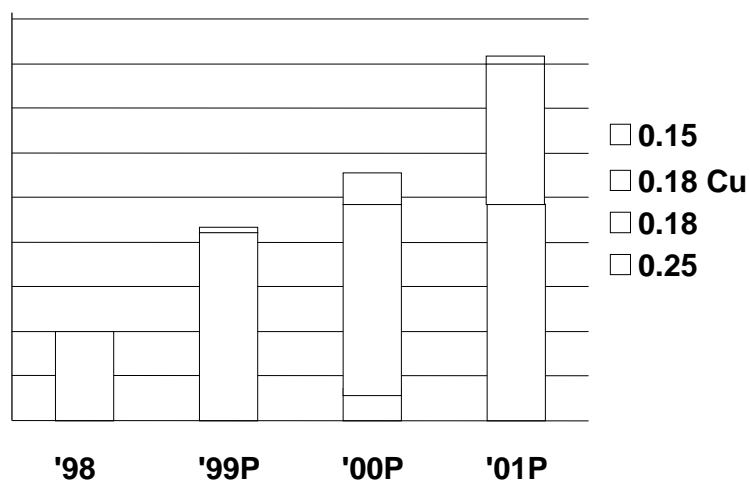
- ◆ **Fab 25, Austin TX**
 - ◆ More than 19M units of AMD-K6® and AMD Athlon™ processors shipped in 1999
 - ◆ 0.18um AMD Athlon Processor status
 - ◆ first production wafers starts in Q3 '99
 - ◆ 100% of AMD Athlon Processor wafer starts are now 0.18um
- ◆ **Fab 30, Dresden Germany**
 - ◆ Initial equipment set installed
 - ◆ 900MHz Copper technology demo in 11/99
 - ◆ On track for first 0.18u copper AMD Athlon processor shipments in mid '00



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Manufacturing Technology & Capacity

Number of Wafers

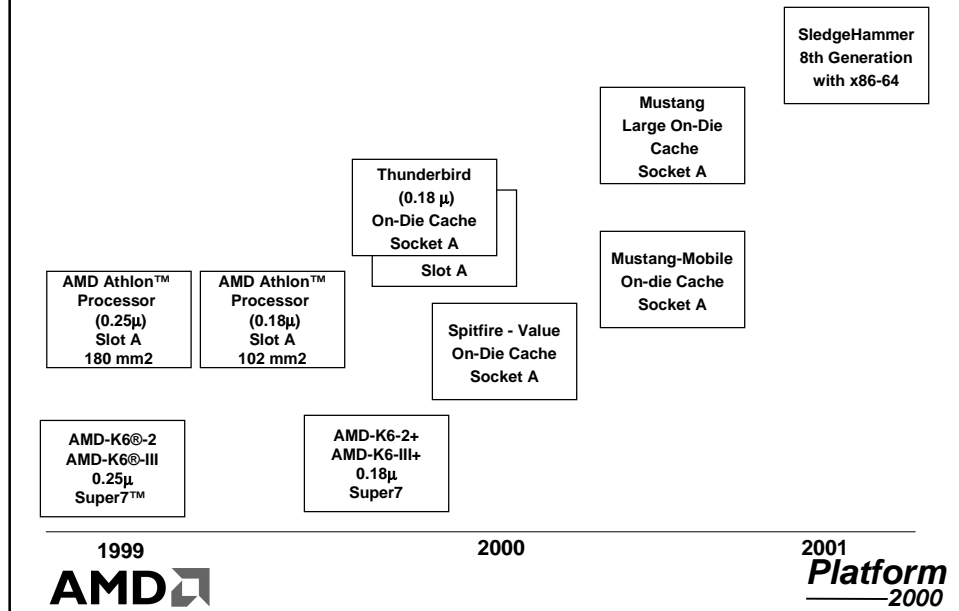


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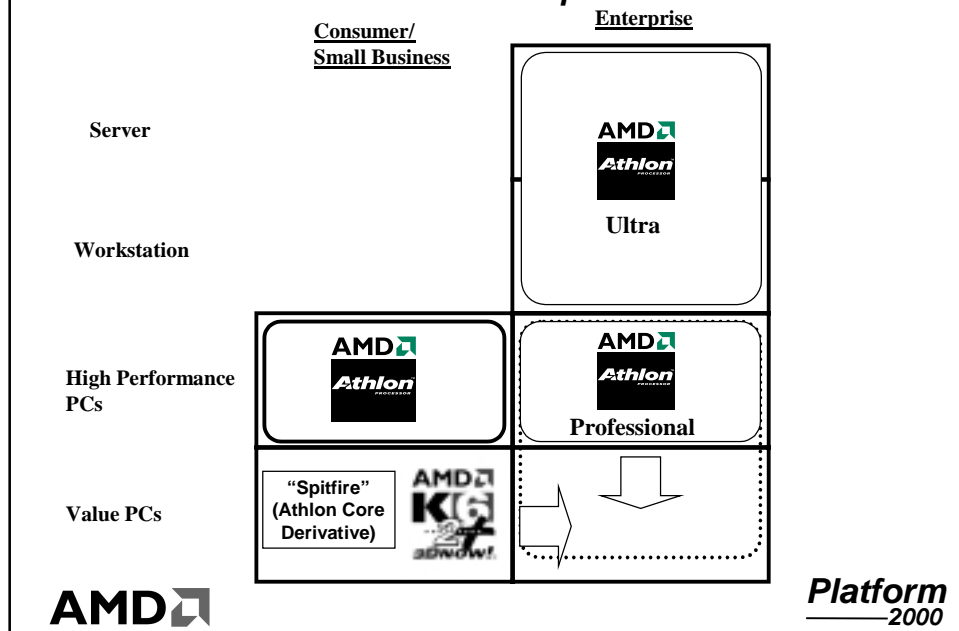
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AMD CPU Cores in 2000-2001



AMD CPU Brand Map '00

Planned Processor Brand Roadmap



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AMD Athlon™ Chipset Roadmap



AMD-750™ Chipset

- Athlon 200 MHz host bus
- PC100
- 2X AGP
- Dual EIDE channels
- 4 port OHCI USB controller
- Hardware SMBUS
- Power Mgmt.
- I/O APIC
- ATA-66

AMD-760™/AMD-770™ Chipsets

- AMD-760 1 processor version
- AMD-770 2 processor version
- Athlon 266/200 MHz host bus
- DDR PC-2100™ & PC-1600™
- Up to 4 DIMMs
- Buffered & Unbuffered DIMMs
- Up to 8GB addressing
- 4X AGP
- 4 port OHCI USB controller
- Suspend-to-RAM
- LPC interface
- Next Generation ATA



Chipset Partners

VIA KX133™ Chipset



- Athlon 200 MHz host bus
- PC-133
- 4X AGP
- ATA-66
- AC97 Audio/Modem
- Hardware Monitoring
- SIO
- Supports AMD Athlon PGA

Future 3rd Party Chipsets



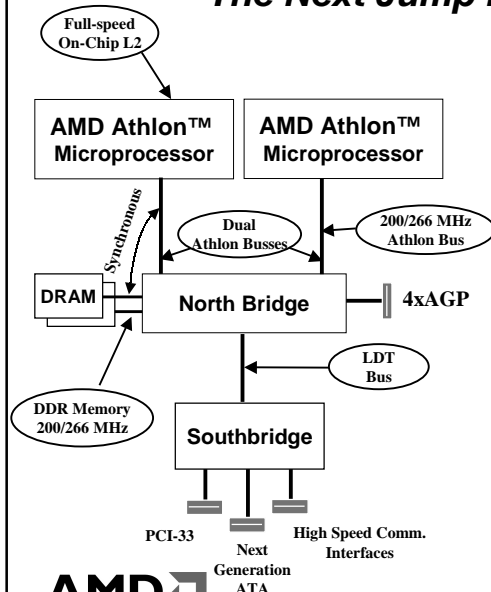
- Will Feature:
- Athlon 200/266 MHz host bus
 - SDRAM PC-133
 - DDR PC-2100 & PC-1600
 - Integrated Graphics
 - high speed NB-SB interface
 - 4X AGP
 - Next Generation ATA
 - Integrated Comm. Cores
 - Security Features



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AMD Athlon™ Platform: The Next Jump in Performance



AMD Athlon

- ◆ On-chip full-speed L2 caches
- ◆ Larger L2 caches
- ◆ Clock Speed

266MHz Front-Side Bus (FSB)

- ◆ AMD will debut a 266MHz FSB in 2000; increasing the bandwidth of our industry leading 200MHz bus by 33%

PC2100 & PC1600 DDR Memory

- ◆ Lowest latency and highest bandwidth (to 2.1 GB/sec) PC memory

Lighting Data Transport™ (LDT)

- ◆ Provides bandwidth and isochronous capability for next generation I/O integration

Multi-Processor

- ◆ True multiprocessor chipset with a dedicated 266MHz Athlon bus per processor
- ◆ Point to point host to northbridge connection enabling higher frequencies and bandwidth



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LDT

The System Bus of the Future



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The System Bus of the Future

Lighting Data Transport (LDT)

What is LDT?

LDT is a new system bus that increases the bandwidth of the system to take full advantage of leading edge AMD Athlon performance. LDT delivers unprecedented bandwidth for chip-to-chip or chip-to-backplane interconnects. LDT can be utilized for either I/O or multiprocessor interconnects.

Why LDT?

LDT improves systems bandwidth to take advantage of the leading-edge performance of AMD Athlon and future processors. LDT enables innovative I/O technologies such as Infiniband system I/O and will provide the system bandwidth necessary for multiprocessor (MP) systems.

Benefits of LDT:

- Improved overall system bandwidth
- "Daisy-chain" feature allows a simple design that adds I/O flexibility through a single data link
- Complements externally visible bus standards (PCI and other cards don't change)

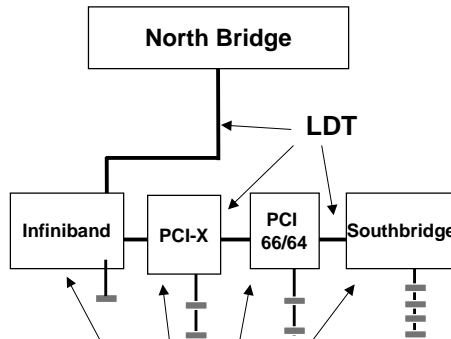


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Daisy Chain Feature Enables Design Flexibility



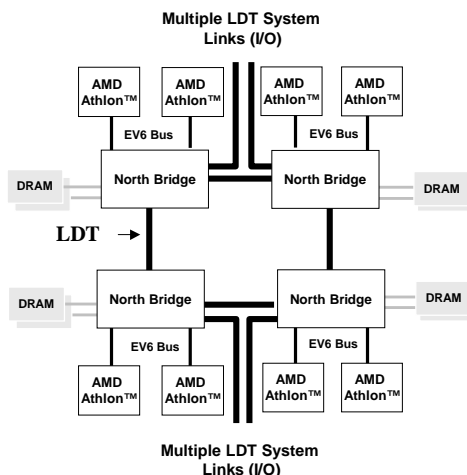
Bridge chips allow all I/O standards to be interchangeable within the system

- Rich I/O bandwidth: up to 3.2 GB/s
- LDT utilizes multiple links through daisy chain feature
 - Bridge chips allow for simple I/O additions
 - Flexibility: Bridge chips can be re-used on other LDT I/O implementations
- LDT complements externally visible bus standards
 - PCI doesn't change
- LDT provides a fast link to Infiniband for server clustering
- Fully Isochronous
 - Guarantees bandwidth for 1394 and streaming video



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Point-to-Point Connections in Multiprocessor Implementations



- Point-to-point connections will have up to 6.4 GB/s bandwidth with LDT.
- Multiprocessor implementations with LDT will be "coherent".
- This multiprocessor (MP) implementation allows for memory and/or I/O capacity and bandwidth to be scaled.



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SledgeHammer™ AMD's Next Generation Processor



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AMD's Eighth Generation Processor: SledgeHammer™

SledgeHammer

- ◆ AMD's eighth generation processor
- ◆ Planned to continue AMD's leadership in x86 performance
- ◆ Planned for 2001 introduction

Key Features

- ◆ Designed for ultra high frequency
- ◆ Core is both 32 and 64-bit capable
- ◆ x86-64™ : A straightforward approach to 64-bit computing
- ◆ Floating Point Enhancements: Enables floating point performance that will compete with even the best RISC processors



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Eighth Generation: x86-64

What is x86-64?

- ◆ x86-64 is AMD's fully compatible solution to extend today's 32 bit x86 instruction set to support 64-bit addresses and data sets

Why go to 64-bit computing?

- ◆ Support for operating systems and applications with large memory requirements (>4 GB). The problem the CIO is trying to solve is that enterprise servers are utilizing extremely large data sets for databases
- ◆ Since the vast majority of applications aren't accessing extremely large data sets, they won't require greater than 4GB addressability, so 64-bit addressing isn't a necessity for most applications

Benefits of x86-64

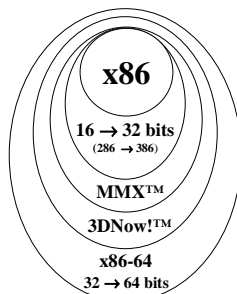
- ◆ Core performance will be state of the art for both 32-bit and 64-bit applications (they are the same core)
- ◆ Allows the 1% of applications that need 64-bit address space to migrate to 64-bit seamlessly and at the user's pace
- ◆ Allows the 99% of applications that never need 64-bit to remain 32-bit and have state-of-the-art performance



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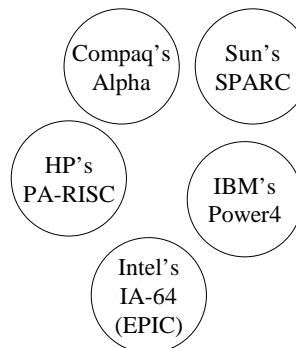
Instruction Sets

X86-64



- AMD's x86-64 strategy is based on an evolution of the current 32-bit x86 architecture
- Just as 32 bits was an extension of x86 with the 386 generation of processors, AMD will extend x86 to 64-bits in SledgeHammer.
- As before, compatibility is retained with the current installed base of x86 operating systems and applications.
- The most straight forward plan to 64-bit path

RISC and IA-64



- There are many 64-bit RISC solutions.
- Each is a unique instruction set compatible only to itself.
- All will require unique OS and application support to utilize large memory addressing



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The Last Diversion: RISC vs CISC

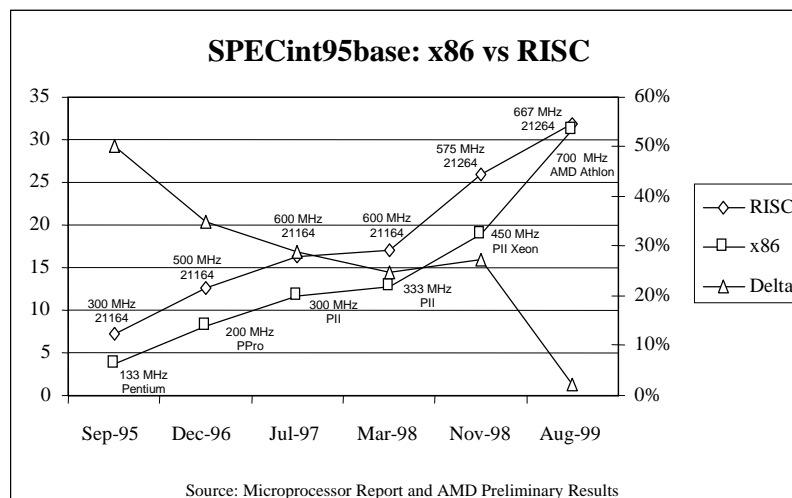
- ◆ RISC (and other) ideas brought to x86
 - ◆ Emphasis on frequency and time to market
 - ◆ Non-microcoded execution
 - ◆ Pipelined execution
 - ◆ Superscalar execution with renaming
 - ◆ Out of order load/store, prefetch
- ◆ The gap has been closed for integer performance
- ◆ The gap will be closed for floating point performance within a generation



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RISC vs x86 Performance

In 4 years x86 performance has nearly erased a 50% SPECint deficit



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AMD Microprocessor Summary

- ◆ **AMD Athlon™ processors and platform are providing performance leadership**
 - ◆ AMD committed to 1GHz in 2000
 - ◆ AMD committed to driving the DDR standard into Athlon™ platforms with AMD-760™ /AMD-770™
 - ◆ LDT will dramatically improve systems bandwidth to take advantage of the leading-edge performance of AMD Athlon™ processor and future processors
- ◆ **SledgeHammer™ will enable the highest levels of 32bit and 64bit platform performance**
- ◆ **AMD Athlon™ platform roadmap will enable expansion into enterprise desktop, server and workstation markets**



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AMD Athlon™ Processor



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